CHI MEI OPTOELECTRONICS CORP.

Issue Date:Jan. 22.2009
Model No.: V546H1-PH5
Approval

TFT LCD Approval Specification

MODEL NO.: V546H1-PH5

Customer: _____

Approved by:_____

Note:

Approved By	TV Head Division
	LY Chen

Reviewed By	QA Dept.	Product Development Div.
	Kc_Ko	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	Wang-Yang Li	Trina Lee

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Jan 22, 2009	All	All	The Approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-PH5 is a 54.6" TFT Liquid Crystal Display cell with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1.073G colors (10-bit/color). The backlight unit is not built-in.

1.2 FEATURES

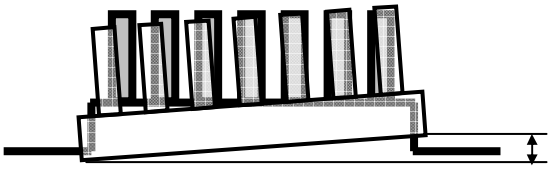
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	54.6
Pixels [lines]	1920 × 1080
Active Area [mm]	1209.6(H) x 680.4(V) (54.6" diagonal)
Sub-Pixel Pitch [mm]	0.21(H) x 0.63(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	3392
Physical Size [mm]	1251.4(W) x 737(H) x 1.75(D) Typ
Display Mode	Transmissive mode / Normally black
Contrast Ratio	4000:1 Typ. (Typical value measured at CMO's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMO's module)
Color Chromaticity	R=(0.655, 0.326) G=(0.299, 0.599) B=(0.147, 0.099) W=(0.333, 0.372) (Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages.)
Cell Transparency [%]	5.6%Typ. (Typical value measured at CMO's module)
Polarizer Surface Treatment	Anti-Glare coating (Super Clear) Hardness (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	3392	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT (BASE ON CMO MODULE V546H1-LH1)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	50	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

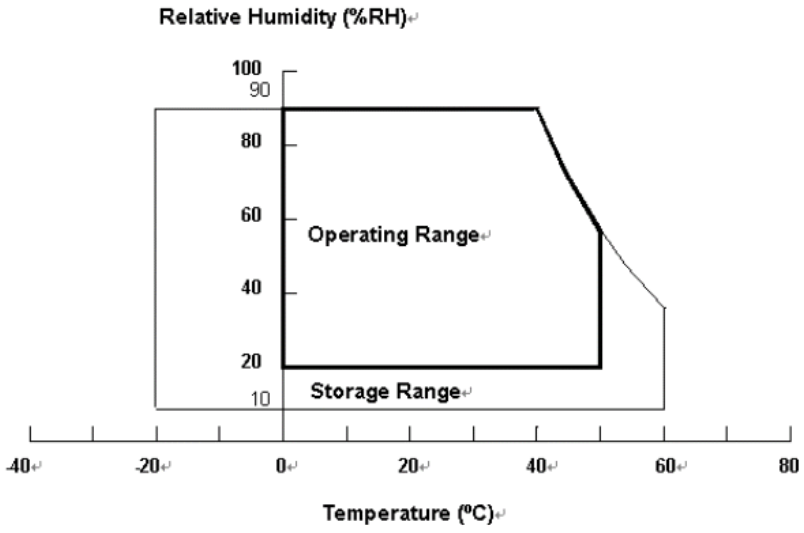
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

Storage condition: With shipping package.

Storage temperature rang: 25±5℃

Storage humidity range: 50±10%RH

Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 ELECTRICAL ABSOLUTE RATINGS (OPEN CELL)

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{AA}	-0.3	17.9	V	(1)
Power Supply Voltage	V_{GHP}	-0.3	32.3	V	
Power Supply Voltage	V_{GL}	-5.7	-0.3	V	
Logic Input Voltage	V_{DD}	-0.3	3.4	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{GH}	31.3	31.8	32.3	V	
		V_{GL}	-5.7	-5.5	-5.3	V	
		V_{AA}	17.5	17.7	17.9	V	
		V_{DD}	3.2	3.3	3.4	V	
Power Supply Current		I_{GH}	-	-	50	mA	
		I_{GL}	-	-	50	A	
		I_{AA}	-	-	1300	A	
		I_{33V}	-	-	2300	A	
CMOS interface	Input High Threshold Voltage	2.7		3.3		V	
	Input Low Threshold Voltage	0		0.7		V	

Note (1) The module should be always operated within the above ranges.

3.2 RSDS CHARACTERISTICS

(Ta = -10 ± 85 ºC)

Item	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
RSDS high input Voltage	$V_{DIFFRSDS}$	V_{CMRSDS} = +1.2V(1)	100	200		mV
RSDS low input Voltage	$V_{DIFFRSDS}$	V_{CMRSDS} = +1.2V(1)		-200	-100	mV
RSDS common mode input voltage range	V_{CMRSDS}	$V_{DIFFRSDS}$ = 200mV (2)	VSSD + 0.1	Note(3)	VSSD + 1.2	V
RSDS Input leakage current	I_{DL}	$D_{XX}P$, $D_{XX}N$, CLKO, CLPN	-10	-	10	μA

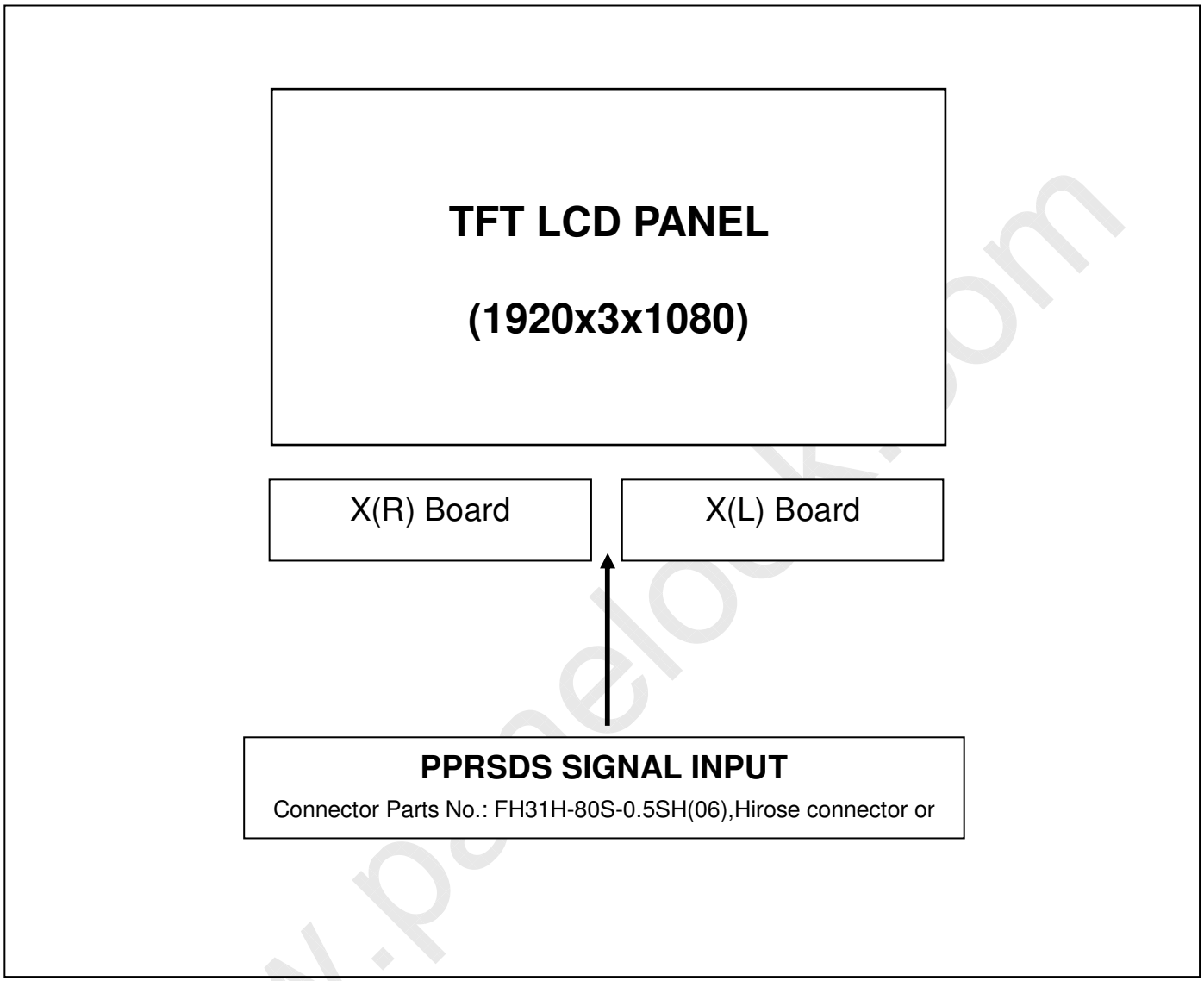
Note (1) V_{CMRSDS} = (VCLKP + VCLKN)/2 or V_{CMRSDS} = ($VD_{XX}P$ + $VD_{XX}N$)/2

Note (2) $V_{DIFFRSDS}$ = VCLKP - VCLKN or $V_{DIFFRSDS}$ = $VD_{XX}P$ - $VD_{XX}N$

Note (3) V_{CMRSDS} = +1.2V(VDDD = 3.3V)

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Pin assignment

CN1(XL) Connector Pin Assignment

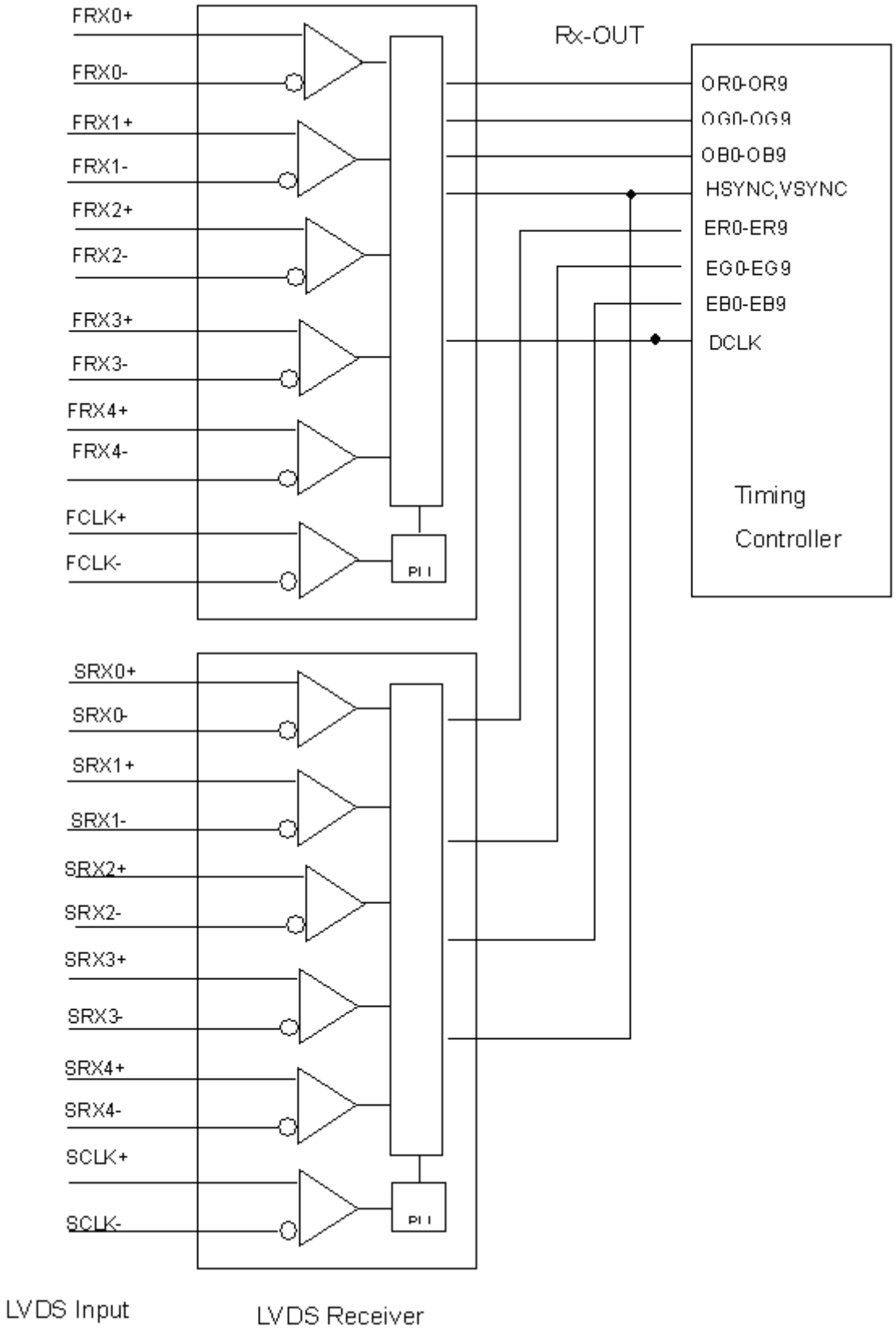
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	GND	Ground	41	AD0M_1	A-Path RSDS data signal
2	BD1P_4	B-Path RSDS data signal	42	GND	Ground
3	BD1M_4	B-Path RSDS data signal	43	GM20	Gamma Power supply
4	GND	Ground	44	GM19	Gamma Power supply
5	N.C.	No connection	45	GM18	Gamma Power supply
6	N.C.	No connection	46	GM17	Gamma Power supply
7	GND	Ground	47	GM16	Gamma Power supply
8	BD0P_4	B-Path RSDS data signal	48	GM15	Gamma Power supply
9	BD0M_4	B-Path RSDS data signal	49	GM14	Gamma Power supply
10	AD1P_4	A-Path RSDS data signal	50	GM13	Gamma Power supply
11	AD1M_4	A-Path RSDS data signal	51	GM12	Gamma Power supply
12	AD0P_4	A-Path RSDS data signal	52	GM11	Gamma Power supply
13	AD0M_4	A-Path RSDS data signal	53	GM10	Gamma Power supply
14	BD1P_3	B-Path RSDS data signal	54	GM9	Gamma Power supply
15	BD1M_3	B-Path RSDS data signal	55	GM8	Gamma Power supply
16	BD0P_3	B-Path RSDS data signal	56	GM7	Gamma Power supply
17	BD0M_3	B-Path RSDS data signal	57	GM6	Gamma Power supply
18	AD1P_3	A-Path RSDS data signal	58	GM5	Gamma Power supply
19	AD1M_3	A-Path RSDS data signal	59	GM4	Gamma Power supply
20	AD0P_3	A-Path RSDS data signal	60	GM3	Gamma Power supply
21	AD0M_3	A-Path RSDS data signal	61	GM2	Gamma Power supply
22	BD1P_2	B-Path RSDS data signal	62	GM1	Gamma Power supply
23	BD1M_2	B-Path RSDS data signal	63	GND	Ground
24	BD0P_2	B-Path RSDS data signal	64	TP1	RSDS data latch
25	BD0M_2	B-Path RSDS data signal	65	CKV	Scan driver clock
26	AD1P_2	A-Path RSDS data signal	66	OE1	Scan driver output enable 1
27	AD1M_2	A-Path RSDS data signal	67	OE2	Scan driver output enable 2
28	GND	Ground	68	STV	Scan driver start pulse
29	A_CLKP	Data driver clock	69	GND	Ground
30	A_CLKM	Data driver clock	70	VDD	Logic Power supply
31	GND	Ground	71	VDD	Logic Power supply
32	AD0P_2	A-Path RSDS data signal	72	VDDA	Driver Power supply
33	AD0M_2	A-Path RSDS data signal	73	VDDA	Driver Power supply
34	BD1P_1	B-Path RSDS data signal	74	VCM	VCM Power supply
35	BD1M_1	B-Path RSDS data signal	75	VCM	VCM Power supply
36	BD0P_1	B-Path RSDS data signal	76	VGL	Driver Power supply
37	BD0M_1	B-Path RSDS data signal	77	VGL	Driver Power supply
38	AD1P_1	A-Path RSDS data signal	78	VGH	Driver Power supply
39	AD1M_1	A-Path RSDS data signal	79	VGH	Driver Power supply
40	AD0P_1	A-Path RSDS data signal	80	GND	Ground

CN2(XR) Connector Pin Assignment

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	GND	Ground	41	BD1M_6	B-Path RSDS data signal
2	VGH	Driver Power supply	42	BD0P_6	B-Path RSDS data signal
3	VGH	Driver Power supply	43	BD0M_6	B-Path RSDS data signal
4	VGL	Driver Power supply	44	AD1P_6	A-Path RSDS data signal
5	VGL	Driver Power supply	45	AD1M_6	A-Path RSDS data signal
6	VCM	VCM Power supply	46	AD0P_6	A-Path RSDS data signal
7	VCM	VCM Power supply	47	AD0M_6	A-Path RSDS data signal
8	VDDA	Driver Power supply	48	BD1P_5	B-Path RSDS data signal
9	VDDA	Driver Power supply	49	BD1M_5	B-Path RSDS data signal
10	VDD	Logic Power supply	50	BD0P_5	B-Path RSDS data signal
11	VDD	Logic Power supply	51	BD0M_5	B-Path RSDS data signal
12	GND	Ground	52	GND	Ground
13	VSCM	VSCM Power supply	53	GM20	Gamma Power supply
14	TP1	RSDS data latch	54	GM19	Gamma Power supply
15	STV	Scan driver start pulse	55	GM18	Gamma Power supply
16	CKV	Scan driver clock	56	GM17	Gamma Power supply
17	OE2	Scan driver output enable 2	57	GM16	Gamma Power supply
18	OE1	Scan driver output enable 1	58	GM15	Gamma Power supply
19	GND	Ground	59	GM14	Gamma Power supply
20	BD1P_8	B-Path RSDS data signal	60	GM13	Gamma Power supply
21	BD1M_8	B-Path RSDS data signal	61	GM12	Gamma Power supply
22	BD0P_8	B-Path RSDS data signal	62	GM11	Gamma Power supply
23	BD0M_8	B-Path RSDS data signal	63	GM10	Gamma Power supply
24	AD1P_8	A-Path RSDS data signal	64	GM9	Gamma Power supply
25	AD1M_8	A-Path RSDS data signal	65	GM8	Gamma Power supply
26	AD0P_8	A-Path RSDS data signal	66	GM7	Gamma Power supply
27	AD0M_8	A-Path RSDS data signal	67	GM6	Gamma Power supply
28	GND	Ground	68	GM5	Gamma Power supply
29	C_CLKP	Data driver clock	69	GM4	Gamma Power supply
30	C_CLKM	Data driver clock	70	GM3	Gamma Power supply
31	GND	Ground	71	GM2	Gamma Power supply
32	BD1P_7	B-Path RSDS data signal	72	GM1	Gamma Power supply
33	BD1M_7	B-Path RSDS data signal	73	GND	Ground
34	BD0P_7	B-Path RSDS data signal	74	AD1P_5	A-Path RSDS data signal
35	BD0M_7	B-Path RSDS data signal	75	AD1M_5	A-Path RSDS data signal
36	AD1P_7	A-Path RSDS data signal	76	N.C.	No connection
37	AD1M_7	A-Path RSDS data signal	77	N.C.	No connection
38	AD0P_7	A-Path RSDS data signal	78	AD0P_5	A-Path RSDS data signal
39	AD0M_7	A-Path RSDS data signal	79	AD0M_5	A-Path RSDS data signal
40	BD1P_6	B-Path RSDS data signal	80	GND	Ground

Note (1) CN1、2 Connector Part No.: FH31H-80S-0.5SH(06),Hirose

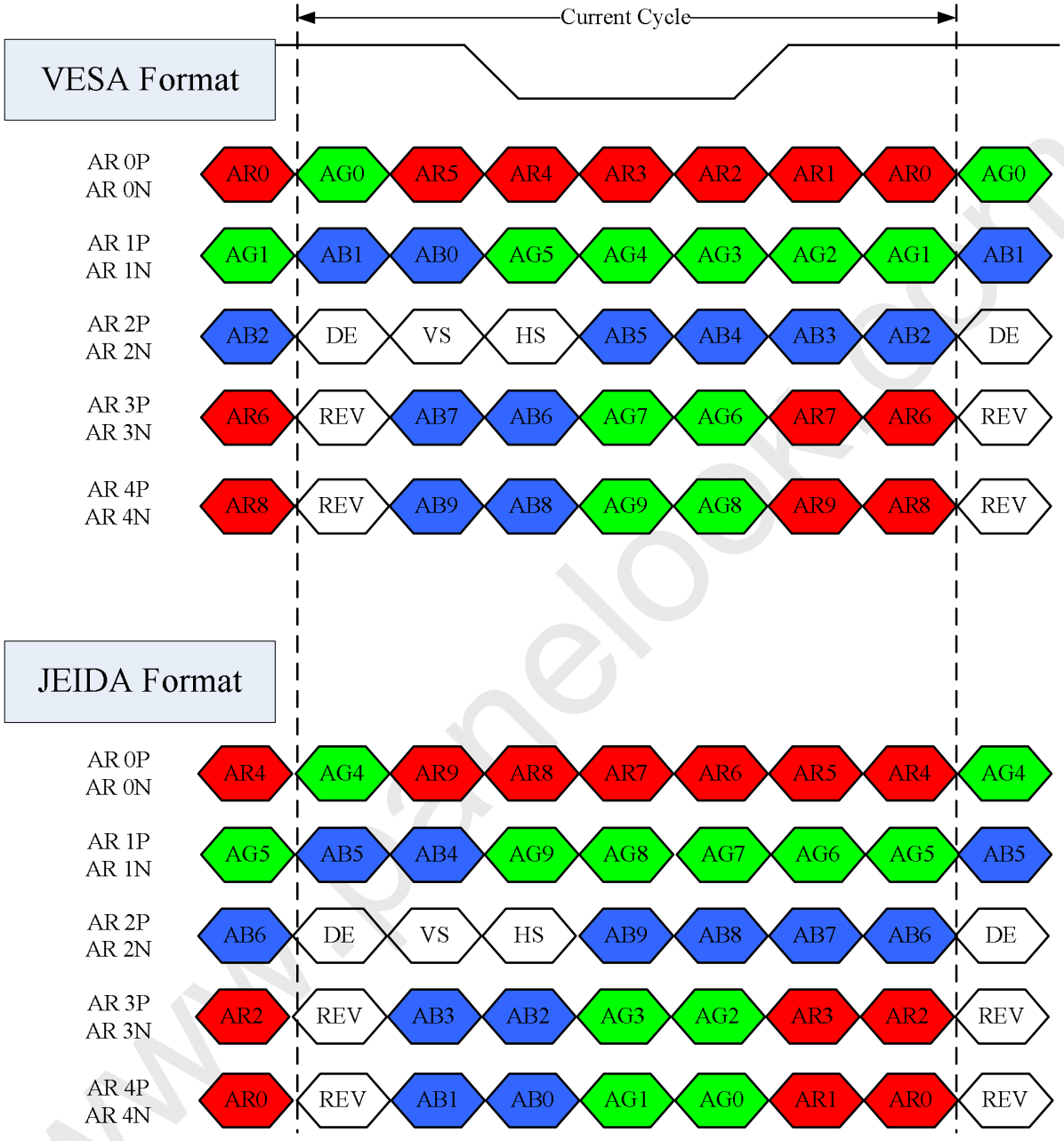
5.2 BLOCK DIAGRAM OF INTERFACE



5.3 LVDS INTERFACE

VESA Format : SELLVDS = H or Open

JEIDA Format : SELLVDS = L



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	-	74	-	MHz	
Hsync		Fh	-	67.5	-	KHz	
Vsync		Fv	-	59.94	-	Hz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	57	60	63	Hz	
	Total	Tv	-	1125	-	Th	Tv=Tvd+Tvb
	Display	Tvd	-	1080	-	Th	-
	Blank	Tvb	-	45	-	Th	-
Horizontal Active Display Term	Total	Th	-	2200	-	Tc	Th=Thd+Thb
	Display	Thd	-	1920	-	Tc	-
	Blank	Thb	-	280	-	Tc	-

6.2 INTERNAL SIGNAL TIMING SPECIFICATIONS(FRC→T-CON)(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

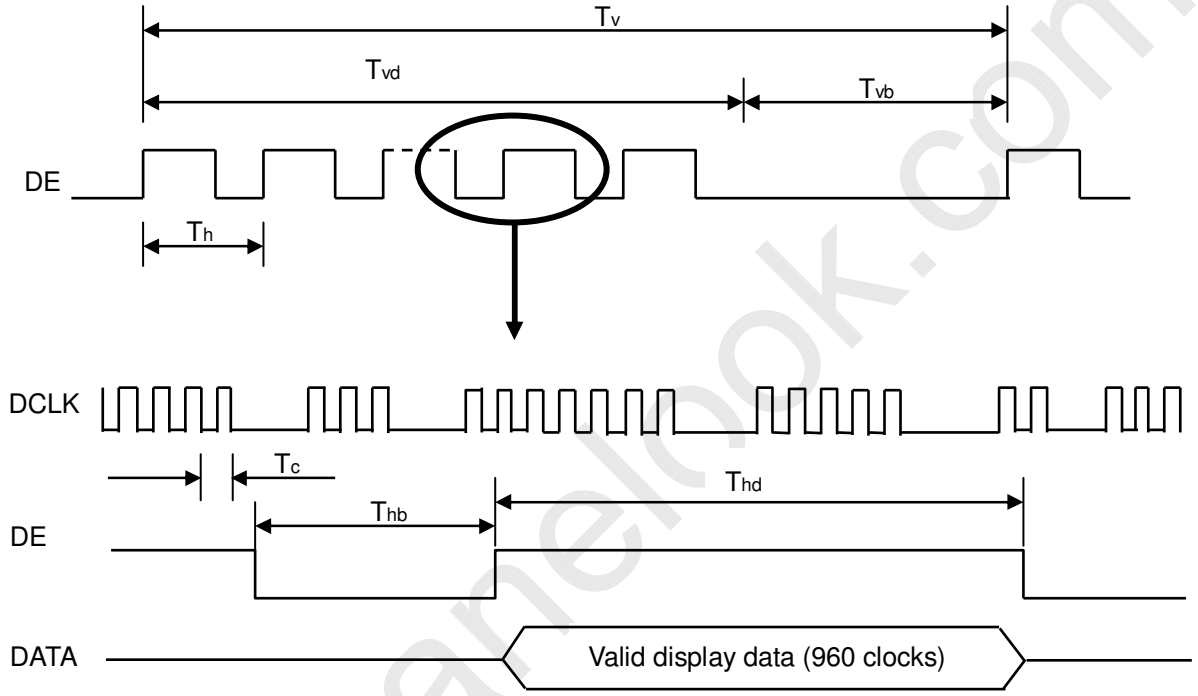
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHz	(1)
Hsync		Fh	-	135	-	KHz	
Vsync		Fv	-	120	-	Hz	
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr6	-	120	-	Hz	
	Total	Tv	1115	1125	1410	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	330	Th	-
Horizontal Active Display Term	Total	Th	540	550	663	Tc	Th=Thd+Thb
	Display	Thd	480	480	480	Tc	-
	Blank	Thb	60	70	183	Tc	-

Note : Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (1) LVDS Clock should not over 80MHz even if H-total or V-total is in spec, and the frequency follows the equation below.

LVDS CLK= Frame rate * H-total * V-total

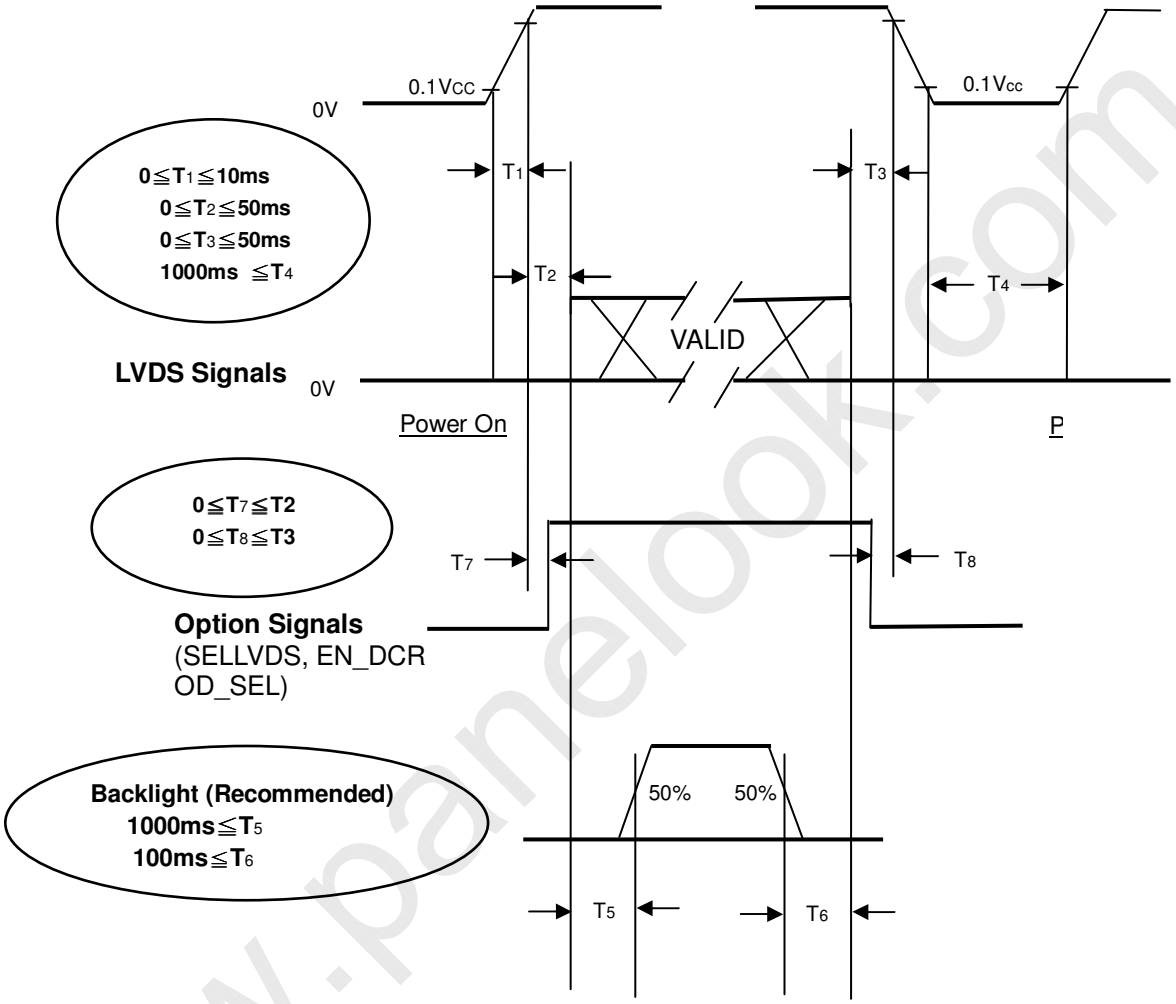
LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	60	Hz

7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (7).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		3000	4000	-	-	(2), (4)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° With CMO Module	-	4	12	ms	(5)
Center Transmittance		T%		-	5.6	-	%	(2), (8)
White Variation		δW		-	-	1.3	-	(2), (7)
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° CS-1000T Standard light source "C"	Typ - 0.03	0.655	Typ + 0.03	-	(1),(6)
		Rcy			0.326		-	
	Green	Gcx			0.299		-	
		Gcy			0.599		-	
	Blue	Bcx			0.148		-	
		Bcy			0.099		-	
	White	Wcx			0.333		-	
		Wcy			0.372		-	
Viewing Angle	Horizontal	θ_x+	CR≥20 With CMO Module	80	88	-	Deg.	(2), (3)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

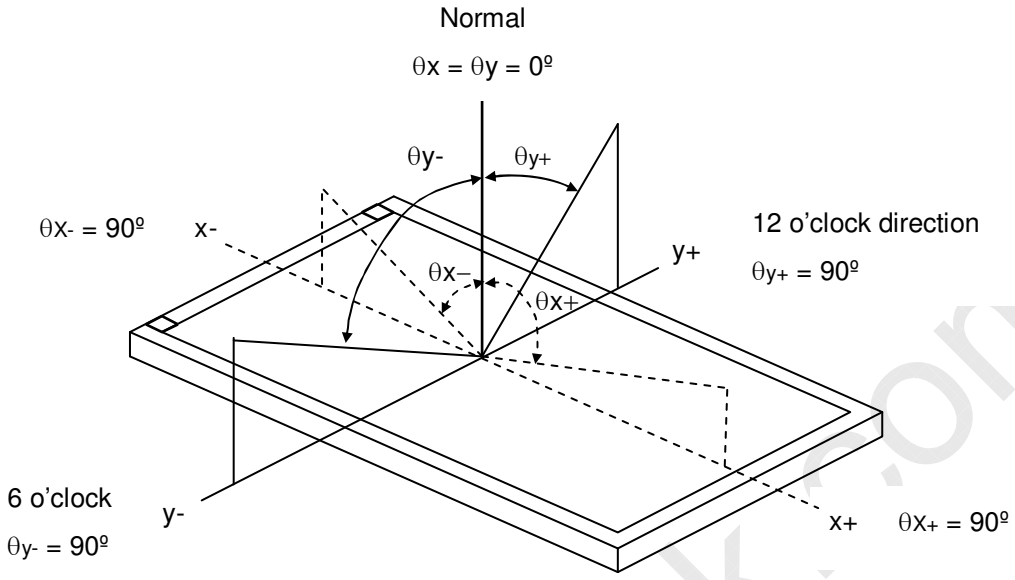
Note (1) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following：

1. Measure Module's and BLU's spectrums. W, R, G, B are with signal input. BLU(for V546H1-LH1) is supplied by CMO.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (2) Light source is the BLU which is supplied by CMO and driving voltages are based on suitable gamma voltages.

Note (3) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by EZ-Contrast 160R (Eldim)



Note (4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

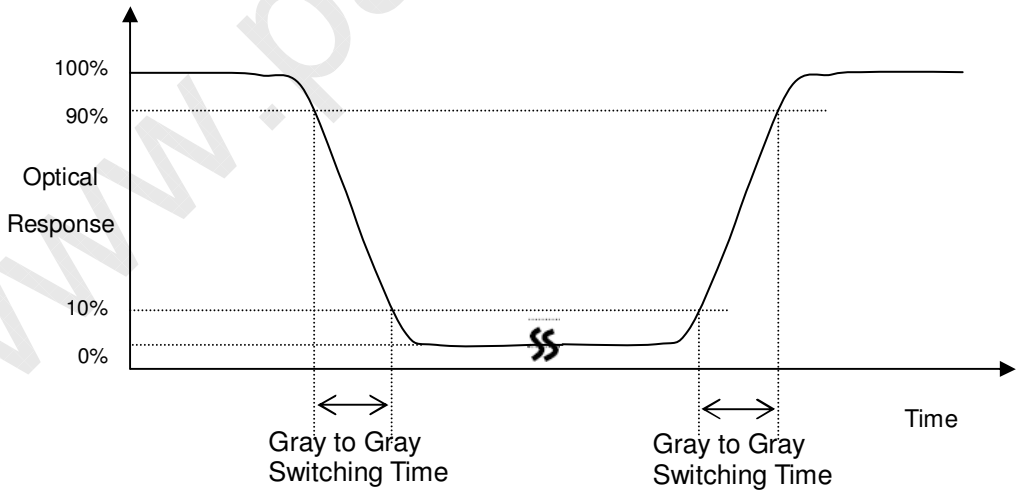
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

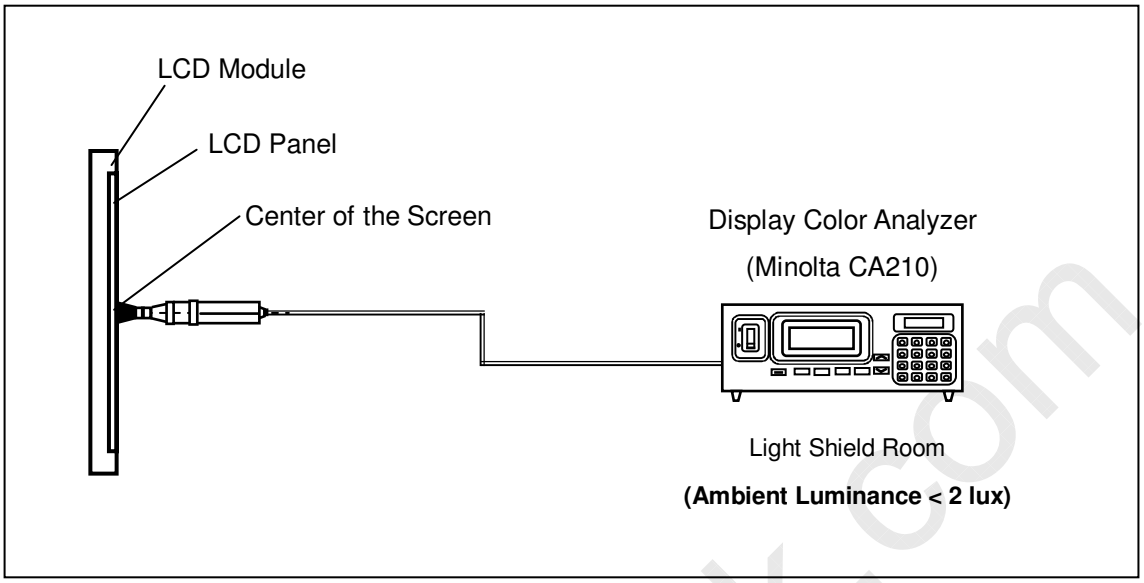
CR = CR (1), where CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (8).

Note (5) Definition of Gray to Gray Switching Time:



Note (6) Measurement Setup:

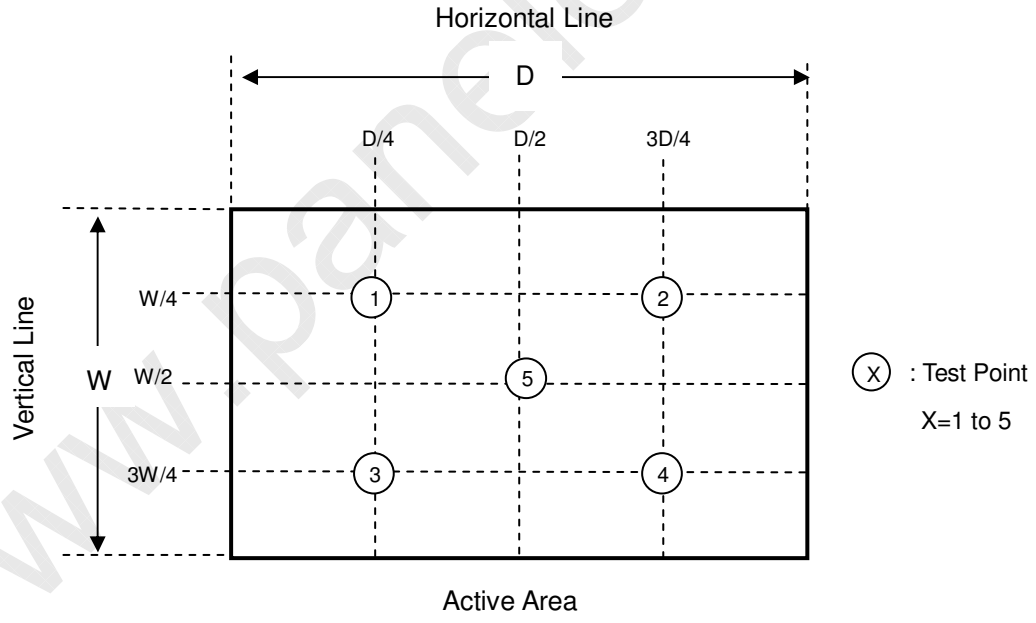
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (8) Definition of Transmittance (T%):

Module is without signal input.

$$\text{Transmittance} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backlight}} * 100\%$$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

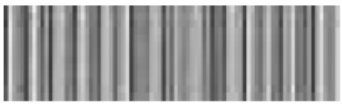
[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMO internal control.

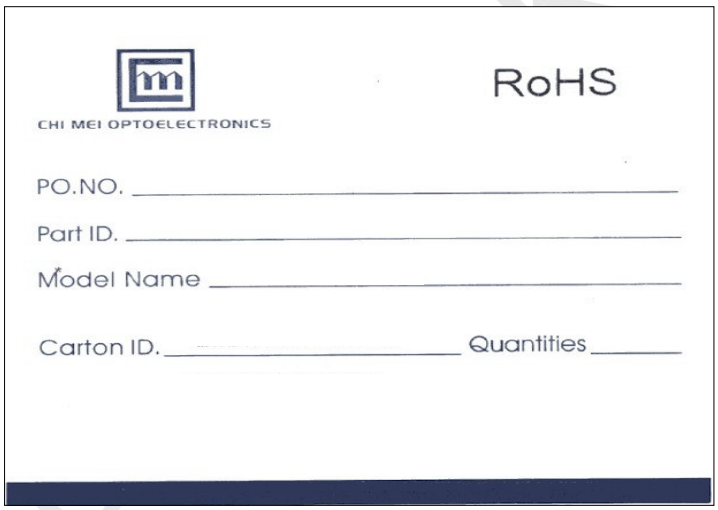
V546H1-PH5



XXXXXXXXXXXXX

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



(a) Model Name: V546H1-PH5

(b) Carton ID: CMO internal control

(c) Quantities: 6 pcs

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 6 LCD TV Panels / 1 Box

(2) Box dimensions : 1454 (L) X 994 (W) X 210 (H)

(3) Weight : approximately 42Kg (6 panels per box)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

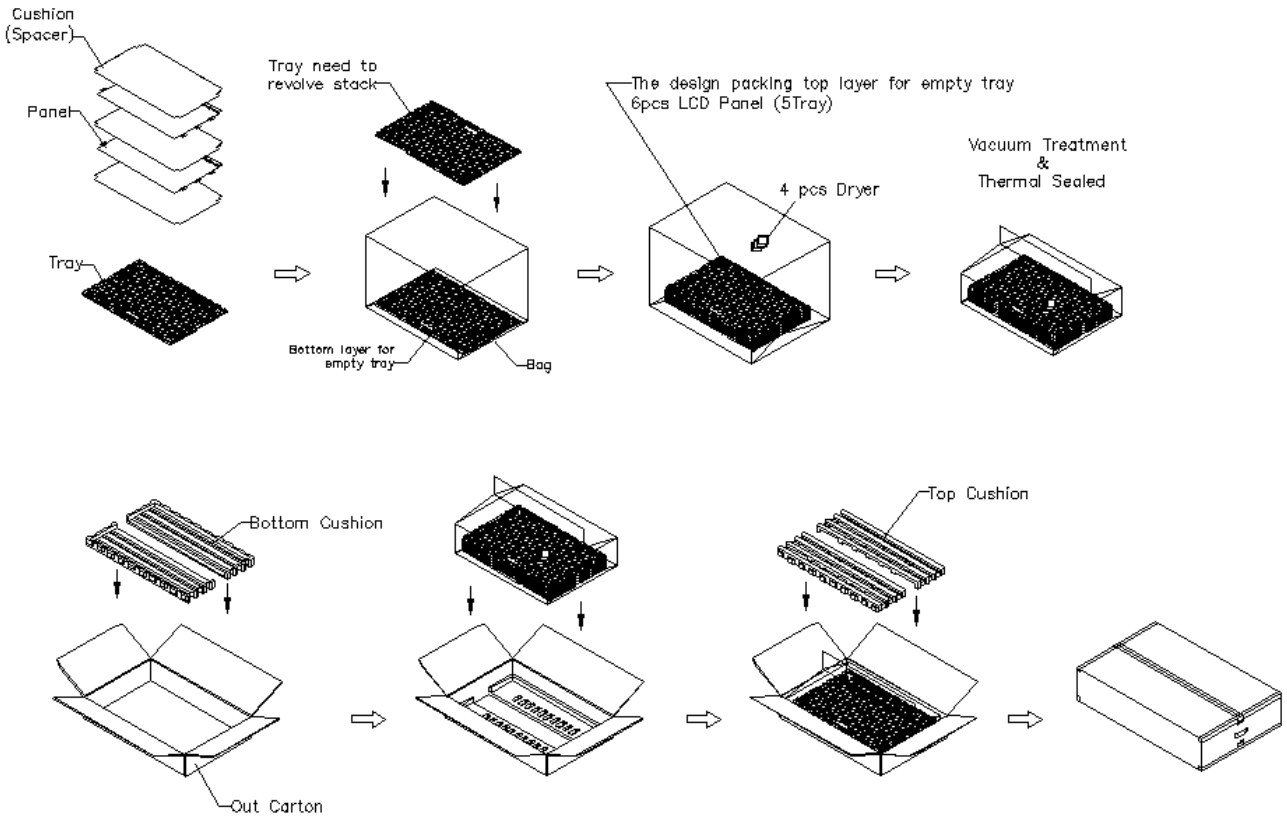
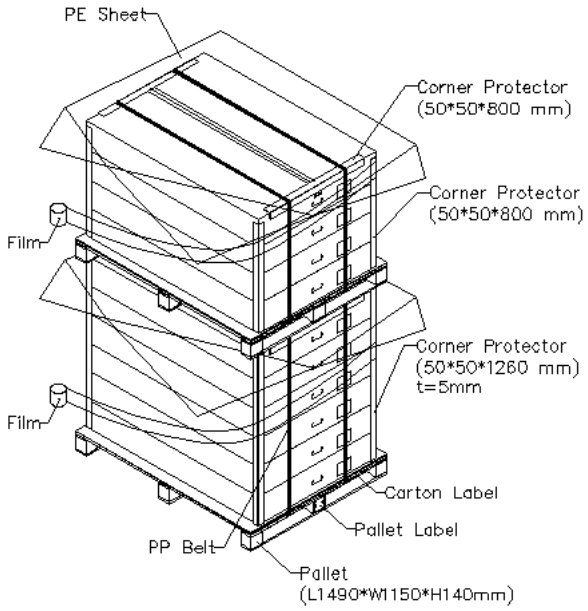
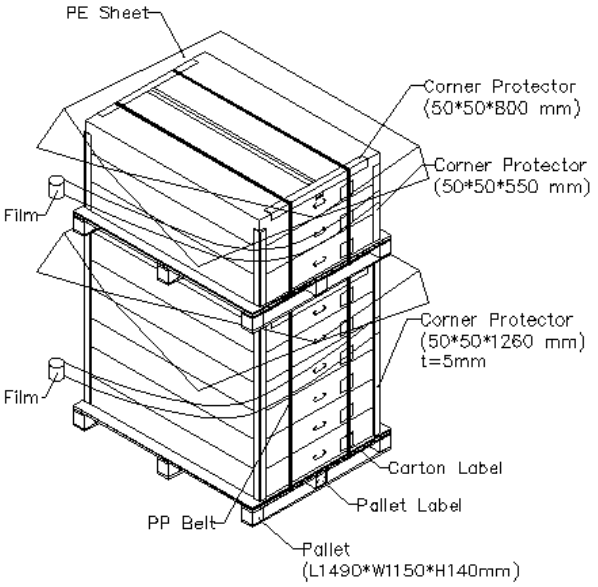


Figure.10-1 packing method

Sea / Land Transportation
(40ft HQ Container)
Gross: 450kg



Sea / Land Transportation
Gross: 408kg



Air Transportation
Gross: 267kg

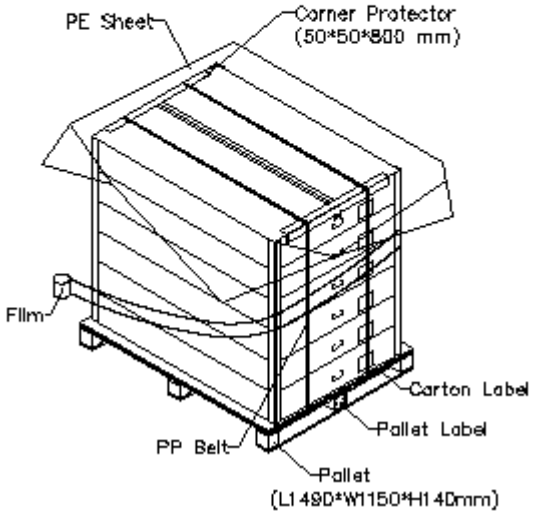


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTICS